Reliability of BGA Packages for Highly Reliable Applications and Chip Scale Package Board Level Reliability

Reza Ghaffarian, Ph.D.
Jet Propulsion Laboratory
California Institute of Technology
Pasadena, California
(626) 354-2059

ABSTRACT

Different aspects of advanced surface mount package technology have been investigated for aerospace applications. Three key areas included understanding assembly reliability behavior of conventional Surface Mount, Ball Grid Arrays (BGAs), and Chip Scale Packages.

Reliability of BGAs were assessed as a part of a consortium led by the Jet Propulsion Laboratory. Nearly 200 test vehicles, each with four packages, were assembled and tested using an experiment design. The most critical variables incorporated in the experiment were package type, board material, surface finish, solder volume, and environmental condition. The BGA test vehicles were subjected to thermal and dynamic environments representative of aerospace applications. The test vehicles were monitored continuously to detect electrical failure and their failure mechanisms were also characterized.

A MicrotypeBGA consortium with industry-wide support was also organized to address technical issues regarding the interplay of package type, 1/0 counts, PWB materials, and manufacturing variables on quality and reliability of board level assembly. This paper will present only the most current thermal cycling test results for plastic BGA packages with 313 and 352 1/0s as well as failure mechanism for ceramic BGA packages with 625 1/0s. The board level reliability of CSP assembly will also be reviewed and projected.

INTRODUCTION

BGA is an important technology for utilizing higher pin counts, without the attendant handling and processing problems of the peripheral leaded packages. They are also robust in processing because of their higher pitch (0.050 inch typical), better lead rigidity, and self-alignment characteristics during reflow processing.

BGAs' solder joints cannot be inspected and reworked using conventional methods and are not well characterized for multiple double sided assembly processing methods. In

high reliability SMT assembly applications, e.g. space and defense, the ability to inspect the solder joints visually has been standard and has been a key factor for providing confidence in solder joint reliability.

To address many common quality and reliability issues of BGAs, JPL organized a consortium with sixteen members in early 1995^[1]. Diverse membership including military, commercial, academia, and infrastructure sectors which permitted a concurrent engineering approach for resolving many challenging technical issues.

Emerging Chip State Packages (CSPs) are competing with bare die assemblies and are now at the stage Ball Grid Arrays (BGAs) were about two years ago. These packages provide the benefits of small size and performance of the bare die or flip chip, with the advantage of standard die packages. Availability of board level solder joint reliability information is critical to the acceptance of CSPs as alternative packages. This paper will present test data and projection for BGA and CSP assembly reliability.

BALL GRID ARRAY PROGRAM

Test Vehicle Configuration

Two test vehicle assemblies included plastic and ceramic packages. Both FR-4 and polyimide Printed Wiring Boards (PWBs) with six layers, .062 inch thick, were used.

Plastic packages covered the range from OMPAC to SuperBGAs (SBGAs). These were:

- Two Peripheral SBGA, 352 and 560 1/0
- . Peripheral OMPAC 352 1/0, PBGA 352 and 256 1/0
- Depopulated full array PBGA 313 I/Os
- . 256 QFP, 0.4 mm Pitch

In SBGA, the IC die is directly attached to an oversize copper plate providing a better heat dissipation efficiency than standard PBGAs. The solder balls for plastic packages were eutectic (63 Sn/37Pb).

Ceramic packages with 625 1/0s and 361 1/0s were also included in our evaluation, Ceramic solder balls with

0.035 inch diameters had a high melting temperature (90Pb/10Sn). These balls were attached to the ceramic substrate with eutectic solder (63 Sn/37Pb). At reflow, package side eutectic solder and the PWB side eutectic paste will be reflowed to provide the electro-mechanical interconnects.

Plastic packages had dummy and daisy chains and the daisy chains on PWB were designed so as to be able to monitor critical solder joint regions. Most packages had four daisy chain patterns, 560 1/0 had five, and QFP had one.

Package Dimensional Characteristics

Package dimensional characteristics are among the key variables that affect solder joint reliability. Dimensional characteristics of all packages were measured using a 3D laser scanning system for solder ball diameter, package warpage, and coplanarity^[2].

Package coplanarity is defined as the distance between the highest solder ball (lead for QFP) and the lowest solder ball. In the 3D laser technique, planarity of individual balls are calculated relative to the seating plane formed from the three tallest balls. Table 1 summarizes planarity results.

Table 1 Planarities of CBGAs & PBGAs

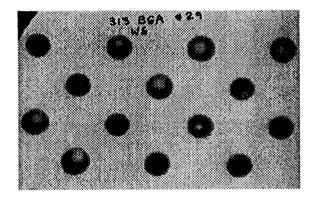
Package Type	Coplanarity Range (inch)
CBGA 625	.0015002 for 104
	0030004 for 4
CBGA 361	.00120022 for 102
5.00 G POA	002 004 6 72
560 SuperBGA	.002004 for 72
	.004006 for 45
	.0060077 for 4
352 SuperBGA	.00140037 for 145
	.00\$8,.0058,.0065,.00
	91
352 OMPAC	.00240057 for 128
,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	·
313 OMPAC	.00220052 for 140
256 OMPAC	.00210047 for 140

Test Vehicle Assembling

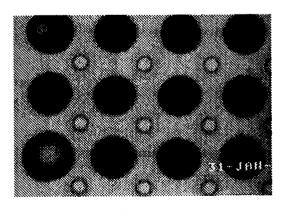
Full assembling was implemented after process optimization from the trial test. The following procedures were followed:

- PWBS were baked at 125°C for 4 hours prior to screen printing.
- 'Iwo types of solder pastes were used, an RMA and a water soluble one.
- Pastes were screen printed and the heights were measured by laser profilometer. Three levels of

- paste were included in evaluation: Standard, high, and low. Stencils were stepped to 50% to accommodate assembling ceramic, plastic, and fine pitch QIP packages in the type 2 test vehicle.
- A 10 zone convection oven was used for reflowing.
- The first assembled Test Vehicle ('1'V) using an RMA reflow process was visually inspected and Xrayed to check solder joint quality.
- All assemblies were X-rayed
- Interchangeability of reflow profile for RMA and Water Soluble (WS) solder pastes was examined. One TV with water soluble solder paste was reflowed using the RMA reflow profile. The solder joints showed much higher void content than expected (Figure 1), as well as signs of flux residues.
- For water soluble paste, a new reflow profile was developed based on the manufacturer's recommendation. This reflow process was used for the remaining test vehicles.
- Figure 2 shows X-ray images when a WS reflow profile was used for the WS solder paste. These joints showed much lower void levels rather than the large voids observed in the former images for the RMA reflow profile of WS paste.

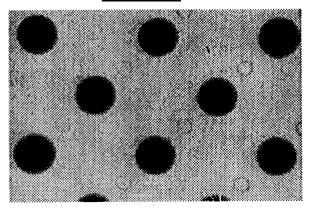


a) Excessive Voids in PBCiA313

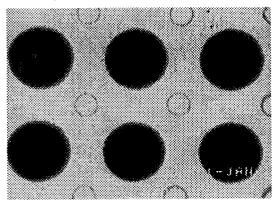


b) Excessive Voids in SBGA352

Figure 1 Excessive Voids for Water Soluble with an RMAReflow Profile



a) Reduced Voids in 313 PBGA



b) Reduced Voids in 352 SPBGA

Figure 2 Voids for Water Soluble Paste with a <u>Water Soluble Reflow</u> Profile

Two test vehicles were assembled:

- Type 1, ceramic and plastic BGA packages with nearly 300 1/0s
- Type 2, ceramic and plastic BGA packages with nearly 600 1/0s. Also utilized was a 256 leaded and a 256 plastic BGA package for evaluating and directly comparing manufacturing robustness and reliability.
- Assemblies with water soluble flux were cleaned in an Electrovert H500. Those with RMAs were cleaned used Isopropyl Alcohol (IPA) and a 5% saponifier.
- All fine pitch QFPs had to be reworked for bridges.

Thermal Cycling

Two significantly different thermal cycle profiles were used at two facilities. The cycle A condition ranged -30 to 100°C and has increase/decrease heating rate of 2°C and dwell of about 20 minutes athortemperature to assure near

complete creeping. The duration of each cycle is **82** minutes.

The cycle B condition ranged -55 to 125°C. It could be also considered a thermal shock since it used three region chamber: hot, ambient, and cold. Heating and cooling rates were non linear and varied between 10 to 15 °C/min. with dwells at extreme temperatures of about 20 minutes. The total cycle lasted approximately 68 minutes. BGA test vehicles were continuously monitored through a LabView system at both facilities.

The criteria for an open solder joint specified in IPC-SM-785, Sect. 6.0, were used as guidelines to interpret electrical interruptions. Generally once the first interruption was observed, there were more than numerous additional interruptions within the 10% of the cycle life. In several instances, one or a few non-consecutive early interruptions were not followed by additional interruptions till significantly later stages of cycling. This was found more with plastic packages.

Damage Monitoring

For conventional SMT solder joint, the pass/fail criteria for high reliability applications relies on visual inspection at 10x to 50x magnifications. For BGA, only edge balls, those not blocked by other components, were visually inspected. A series of single assemblies cut from the test vehicles were used for both visual and SEM inspection to better define visual criteria for acceptance of solder joints as well as monitoring damage progress under different cycling environments.

Figure 3 shows representative SEM and cross-sectional micrographs for a CBGA 625 after 348 cycle A conditon. Cross-section photos are for the perimeter balls, two comers and a center ball. SEM photos for package and board sides of a comer (maximum Distance to Neutral Point(DNP)) and the edge center ball also included.

For B cycle ceramic packages failed at the package interface with signs of significant creeping, and solder grain growth^[2]. The board side solder creeping and cracking were much milder.

Thermal Cycling Results

PBGA 313 and SBGA 352/A & B Cycles

Figure 4 shows cycles to first failure for PBGA 313 and SBGA 352 subjected to B cycle. for assemblies on polyimide and FR-4 PWBs. The most current PBGA 313 assemblies that failed under cycle A condition are also included in the plots for comparison. These assemblies include those reflowed with low, standard, and high solder paste levels.

The cycles to failure were ranked from low to high and failure distribution percentiles were approximated using median plotting position, $F_i = (i-0.3)/(n+0.4)$. Weibull parameters will be generated when all failure data are gathered.

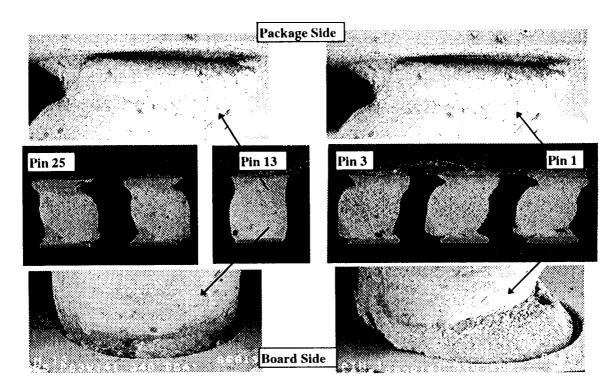


Figure 3 SEM and Cross-section photos for CBGA 625 after 348 cycles (-30°C to 100"C)

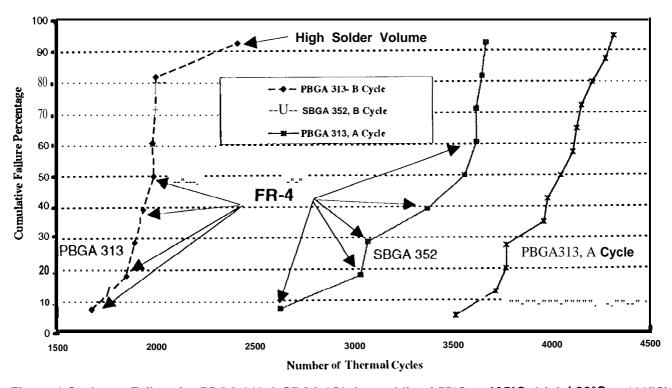


Figure 4 Cycles to Failure for PBGA 313 & SBGA 352 Assemblies (-55°C to 125°C, A) & (-30°C to 100"C)

CSP BOARD LEVEL RELIABILITY

Introduction

Emerging Chip Scale Packages (CSPs) are competing with bare die assemblies and arc now at the stage Ball Grid Arrays (BGAs) were about three years ago. These packages provide the benefits of small size and performance of the bare die or flip chip, with the advantage of standard die packages.

CSPS are defined as packages that are up to 1.2 or 1.5 times larger than the perimeter or the area of the die, respectively. Many manufacturers now refer to CSPS as packages that are the miniaturized version of their previous generation. Packaging accomplishes marry purposes, including the following:

- Provides solder balls and leads that are compatible with the PWB pads for reflow assembly processes, whereas aluminum pads do not.
- Redistributes the tight pitch of the dic to the pitch level that is within the norm of PWB fabrication. The small sizes of CSPS do not permit significant redistribution

- and the current cost effective PWB fabrication limits full adoption of the technology, especially for high 1/0 counts
- Protects the die from physical and alpha radiation damages, and provides a vehicle for thermal dissipation and ease of die functionality testing.

CSPS generally have been categorized based on their fundamental structures. These are:

- Interposer packages with either flex or rigid substrate . Wafer level molding and assembly redistribution
- Lead On Chip (LOC) packages.

Currently, most of data are those that were generated for package qualifications by manufacturers with very limited published information available on assembly reliability^[3].. These data are of limited value to the end user since often they have been collected under significantly different manufacturing and environmental conditions or for packages with different pin counts,

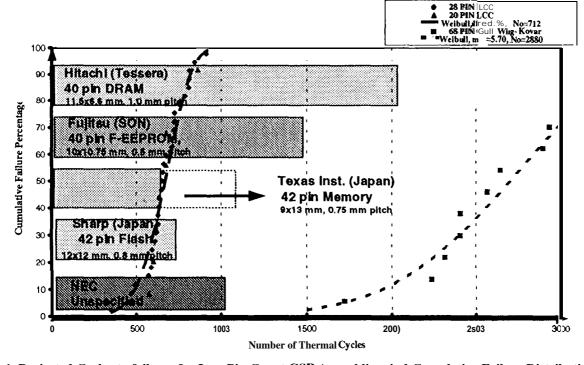


Figure 1. Projected Cycles to failures for Low Pin Count CSP Assemblies rind Cumulative Failure Distributions for Conventional SM Package Assemblies Tested at JPL (-55°C to 100"C)

Assembly Reliability for Conventional Packages and Those Projected for CSPS

Reliability of conventional SM packages as well as Ball Grid Arrays have been investigated at JP1.. Cycles to

failure test data points and their Weibull distributions for 28-, and 20-pin I.CC, and 68-pin gull wing assemblies are shown in Figure 1. Thermal cycling ranged from -55°C to 100°C with 246 minute duration. The failure distribution percentiles were approximated using a median plotting

position, Fi = (i-0.3)/(n+0.4). The two-parameter Weibull cumulative failure distribution was used to fit data.

For comparison, projected cycles to failure for low count CSPs are also included. Results arc those gathered from literature and projected based on a modified Coffin-Manson relationship.

Consortium to Assess CSPs' Board Level Reliability

For wider applications of this CSP technology, the potential user wiii need design reliability data for its design since often they have no resources, time, or ability to perform complex environmental characterizations. JPL has formed a consortium with the objectives of addressing many technical issues regarding the interplay of package type, 1/0 counts, PWB materials, surface finish, and manufacturing variables for the quality and reliability of assembly packages

Currently, the JPL-led MicroypeBGA consortium has defined packages for the test vehicles and is in the process of designing of the test vehicles. It is anticipated that more than 300 test vehicles will be assembled and subjected to various environmental conditions representative of space and military as well as commercial applications.

CONCI, US10NS

BGA Packages and Assembly Reliability

- Planarity levels dependent on package types, but irrespective of package types they decrease as the size decreased.
- Ceramic packages showed lower warpages and were more coplanar than their PBGA counterparts. Numerous ceramic packages had tilted solder balls.
- . Solder ball planarities were significantly higher for plastic than for ceramic packages. A few PBGAs showed unexpectedly higher values above their norm distribution. PBGAs, however, are more robust and the large planarity values might not be as detrimental to their solder joint reliability as those for ceramics. Some planarity differences among the PBGA balls are accommodated by their collapses during the reflow process. This is not the case for CBGAs where high melt solder balls remain intact during reflow. The solder ball diameter controls the stand-off height which is a key factor to solder joint reliability.
- 3D laser scanning is excellent for characterization of package dimensions, but possibly not for solder ball measurement.
- The BGA assembly void levels were the same as those generally observed by industry. As expected, BGAs

- were robust in assembling compared to the 256 fine pitch, 0.4 mm QIPs. Ail QIPs showed bridging to some degree and had to be reworked.
- RMA and water soluble reflow profiles evaluated in this study were significantly different and they were to be optimized separately for the applications. Large rather smaller and sporadic voids were generated when an RMA reflow profile for a water soluble solder paste was used.
- As expected, ceramic packages failed much earlier than their plastic counterparts because of their much larger CTE mismatch on FR-4/Polyimide boards.
 Cycles to electrical failure depended on many parameters including cycle temperature range and package size (1/0).
- Ceramic packages with 625 1/0s were first to show signs of failure among the ceramic (CBGA 361) and plastic packages (SBGA 560, SBGA 352, OMPAC 352, and PBGA 256) when cycled to different temperature ranges.
- Joint failure mechanisms for assemblies exposed to two cycling ranges at two facilities were different. Ceramic assemblies cycled in the range of -30°C to 100°C showed cracking initially at both interconnections with final separation generally from the board side through cutectic solder. The board side joint showed signs of pin hoie formation prior to cracking and complete joint failure. This failure mechanism is similar to those reported in literature for 0°C to 100°C thermal cycles.
- "The PBGAs with 313 1/0, depopulated full arrays, were first among the PBGAs to fail at both cycling ranges. It has been well established that this configuration with solder bails under the die is not optimum from a reliability point of view.
- Solder volume is generally considered to have negligible effect on plastic package assembly reliability. One PBGA 313 package that was assembled with high solder paste volume under cycle B exposure showed the highest number of cycles to failure. This will be assessed when data for cycle A become available.
- The 352 SBGA with no solder bails under the die showed much higher cycles to failure than the PBGA 313 when subjected to cycle B condition.
- For cycle B conditions, plastic package assemblies, PBGA 3 i 3 and SBGA 352 on polyimide, generally failed at a higher number of cycles than those on FR-4.

CSP Assembly Reliability

• The boardlevel reliabilities of most CSP packages are comparable or better than their LCC with a similar 1/0

- counts. These packages, however, **are** not as **robust** as leaded packages including gull wing and J-leads.
- Board level solder joint reliability information is critical to the acceptance of CSPS as alternative packages. It is the objectives of JPL-led MicrotypeBGA consortium to help in developing this aspect of technology infrastructure.

REFERENCES

- 1. R. Ghaffarian, "Area Array Technology Evaluation for Space and Military Applications", <u>The 1996 International Flip Chip</u>, <u>Ball Grid Array</u>, <u>TAB and Advanced Packaging Symposium Proceeding</u>, Feb. 13-16, 1996.
- 2. R, Ghaffarian, "CBGA/PBGA Package Planarity and Assembly Reliability", The 1997 International Flip Chip. Ball Grid Array, TAB and Advanced Packaging Symposium Proceeding, Feb. 17-19, 1997.
- 3. R. Ghaffarian, N. Kim, "Ball Grid Reliability Assessment for Aerospace Applications," <u>30th International Symposium on Microelectronics</u>, Philadelphia, Oct. 12-16, 1997
- 4. R. Ghaffarian, "A Review of Chip Scale Package Assembly Reliability," The Second International

<u>Conference on Chiu-scale Packaging (CHIPCON'97)</u>, Feb. 20-21, 1997

5. R. Ghaffarian, "The Interplay of Solder Joint Quality and Reliability for Leaded and Leadless Components," Ninth Annual Soldering Technology for Electronic Packaging Symposium, Oct. 21-25, 1996, Binghamton, NY

ACKNOWLEDGMENTS

The research described in this publication is being carried out by the Jet Propulsion Laboratory, California Institute of Technology, under a contract with the National Aeronautics and Space Administration,

I would like to acknowledge the in-kind contributions and cooperative efforts of BGA consortium team members and (hose who had been or are being contributors to the progress of program.

My deepest appreciation to P. Barela, K. Bonner, S. Walton, *JPL*; Dr. N. Kim, *Boeing*; M. Simeus, *HMSC*; I. Sterian, *Celestica*; M. Ramkumar, *RIT*; M. Andrews, *ITRI*; S. Levine, *Altron*; P. Mescher, *AMKOR*; M. Cole, A, Trivedi, *IBM*.